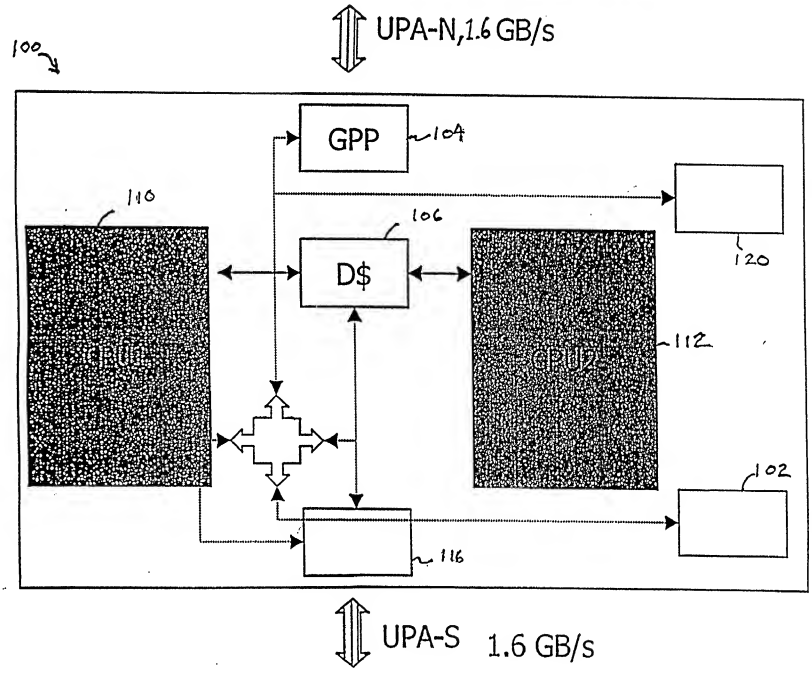
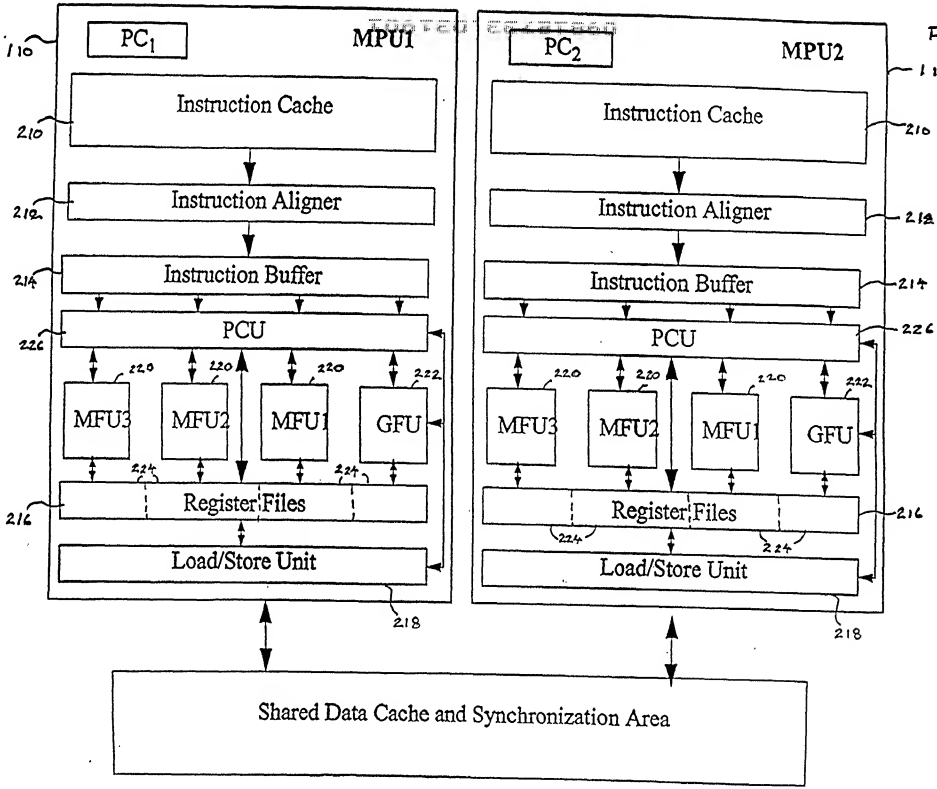
FIG. 1



Title: EFFICIENT HANDLING OF A LARGE REGISTER FILE FOR CONTEXT SWITCHING
Inventors: Marc Tremblay; William Joy
Docket No.: SP-2612-1C US

FIG. 2



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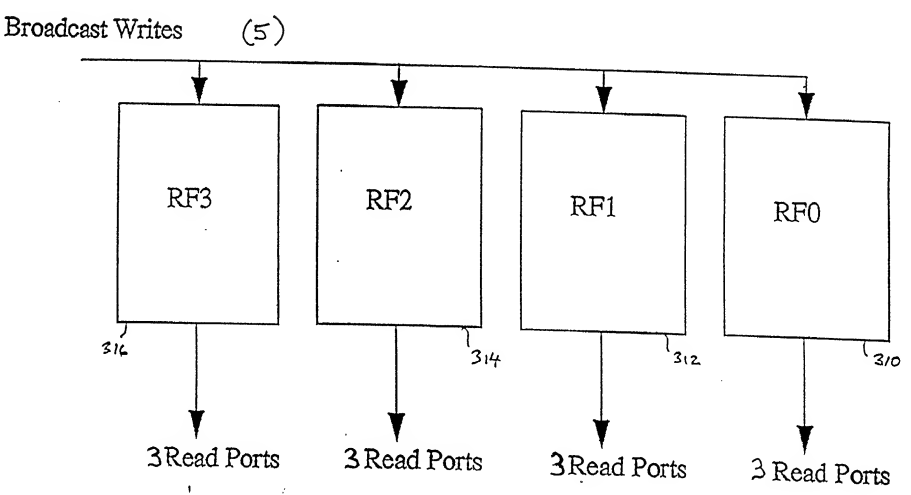


FIGURE 3 .Logical register file physically spit in four coherent parts.

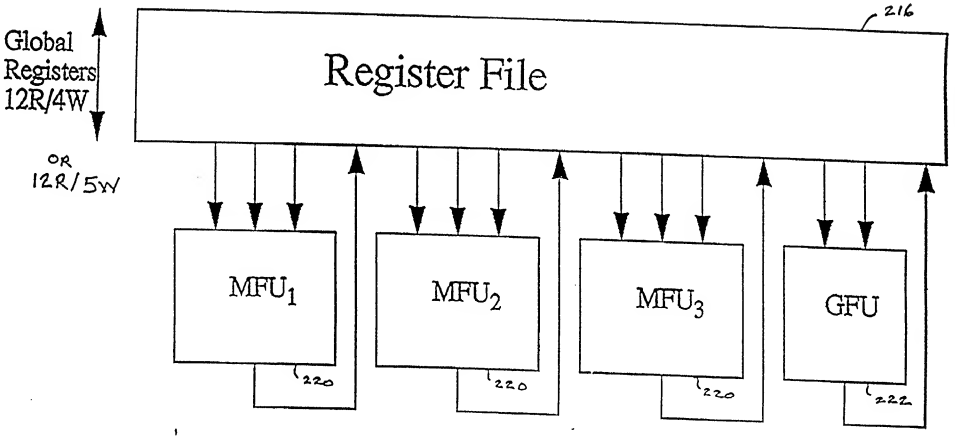


FIGURE 4 .Logical view of the register file to the compiler/programmer.

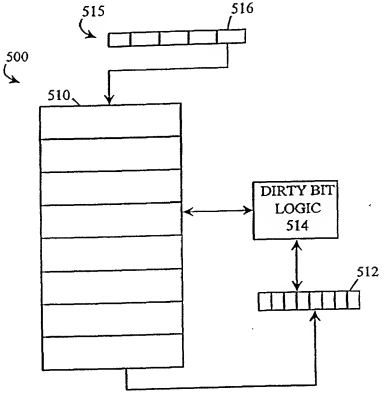


FIG. 5

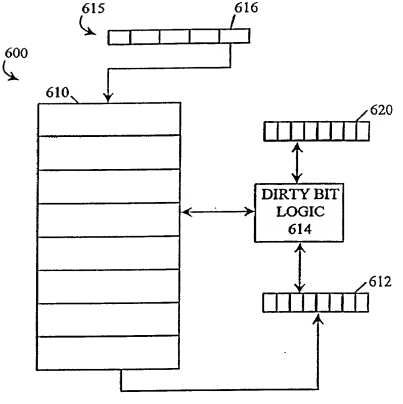
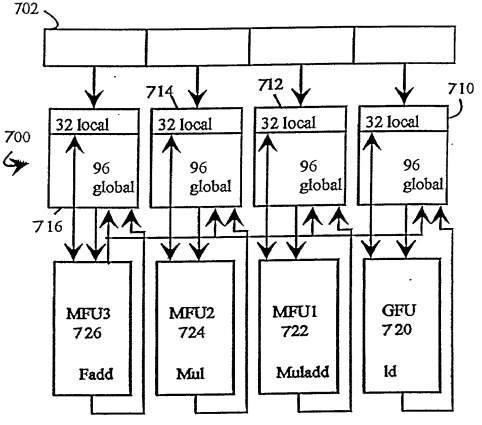


FIG. 6

FIG. 7


702
714
712
710
700
32 local
96 global
716
MFU3 726 Fadd
MFU2 724 Mul
MFU1 722 Muladd
GFU 720 Id

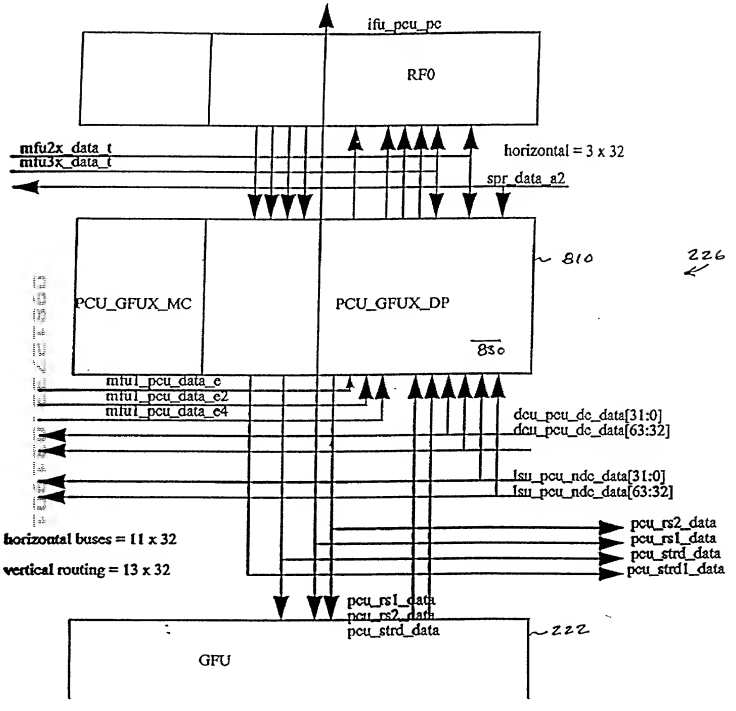


FIGURE 8A Channel congestion above and below pcu_gfux_dp block

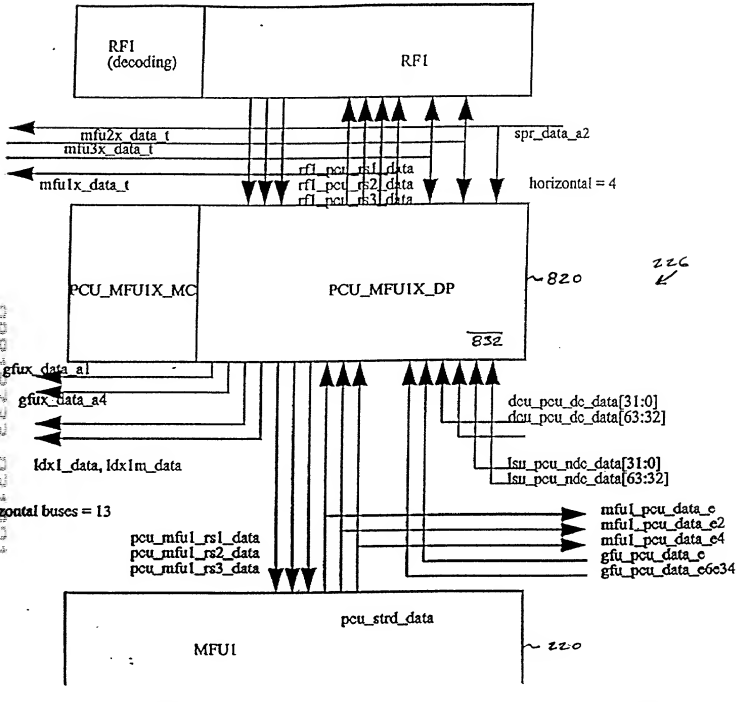


FIGURE 8 8 Channel congestion above and below pcu_mfu1x_dp block

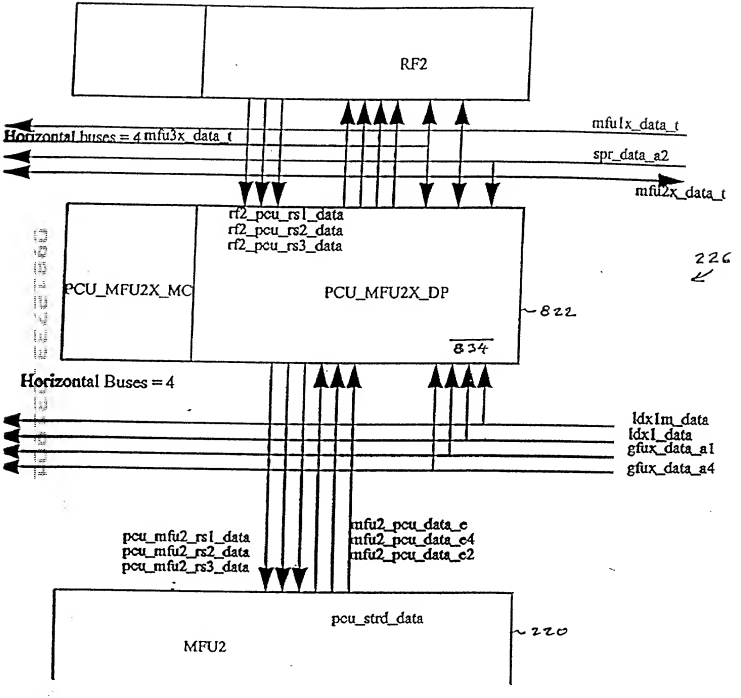


FIGURE 8C Channel congestion above and below pcu_mfu2x-dp block

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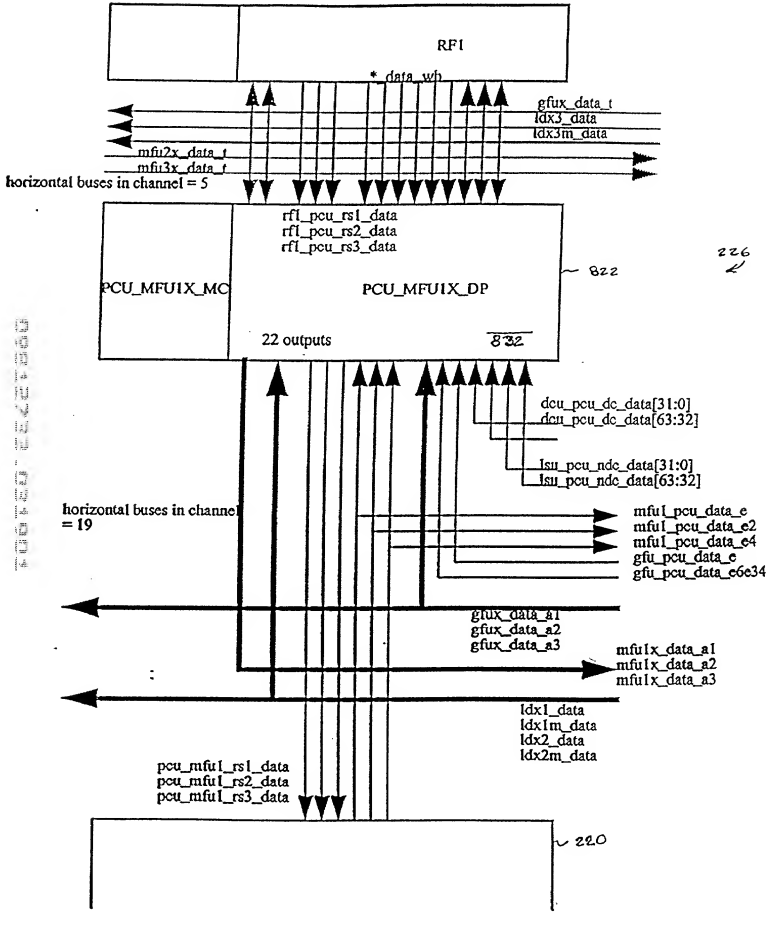
FIG. 8D



Internal Registers of PCU

Register name	width	address specifier	user access	supervisor access	thread state
PSR	8	010_0001	no	rd/wr	yes
TPSR1	8	010_0010	no	,,	yes
TPSR2	8	010_0011	no	,,	yes
PCR	7	010_0000	no	,,	no
TL	2	010_0100	no	,,	no
TICK	32	010_0101	read only	,,	no
TVALUE	32	010_0110	no	,,	no
TCNTL	8	010_0111	no	,,	no
GX	13	001_0000	no	rd only	yes
INT	7	010_1000	no	rd/wr	yes
FSR	16	001_0001	rd/wr	,,	yes
FMT	2	010_1010	rd/wr	rd/wr	yes
DIRTY	6	010_1011	rd/wr	,,	yes
INT_OTHER	-	010_1001	no	wr only	yes

FIG. 9

Processor Control Register (PCR)

PCR	PCR	Description	Initial value	After a trap
[0]	POW	power management	0 (off)	N/C not changed
[1]	ICE	icache enable	0	"
[2]	DCE	dcache enable	0	"
[3]	BPTE	branch predict taken enable	0	"
[4]	PE	pipeline enable	0	"
[5]	MSTEP	memory step	0	"
[6]	PID	processor ID	hard-wired	hardwired

FIG. 10

Instruction vliw_1	Instruction setir ra, PSR
vliw_2	ld_2 [r1+r2], r3
vliw_3	ld_3
vliw_4	ld_4
vliw_5	ld_5
vliw_6	ld_6

FIG. 11A

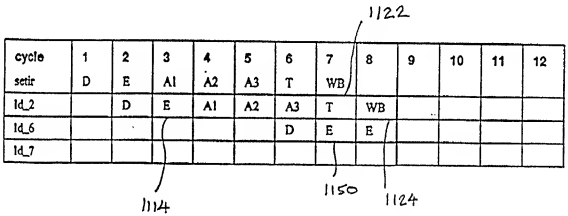


FIG. 11B

Title: EFFICIENT HANDLING OF A LARGE REGISTER FILE FOR CONTEXT SWITCHING
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Instruction	Instruction
vliw_1	setir ra, PCR
vliw_2	inst2
vliw_3	inst3
vliw_4	inst4
vliw_5	inst5
vliw_6	inst6
vliw_7	inst7
vliw_8	inst8
vliw_9	setir rb, PSR
vliw_10	inst10
vliw_11	inst11

FIG. 12A

1212 1222

cycle	1	2	3	4	5	6	7	8	9	10	11	12	13
setir	T	WB											
inst7		D	D	E	A1	A2	A3	T	WB				
inst8				D	D	D	D	D	D	D	E	A1	A2
setir											D	D	D
iST		ST		ST	ST	ST	ST	ST	ST		ST	ST	ST

FIG. 12B

1254

cycle	14	15	16	17	18	19	20	21	22	23	24	25	26
inst8	A3	T	WB										
setir	D	D	D	D	E	A1	A2	A3	T	WB			
inst10					D	D	D	D	D	D	E	A1	A2
inst11											D	E	A1
ST	ST	ST	ST		ST	ST	ST	ST	ST				

Dirty Register 1300

	Unit	rd [6:5]
[0]	all	01
[1]	all	10
[2]	gfu	11
[3]	mfu1	11
[4]	mfu2	11
[5]	mfu3	11

FIG. 13

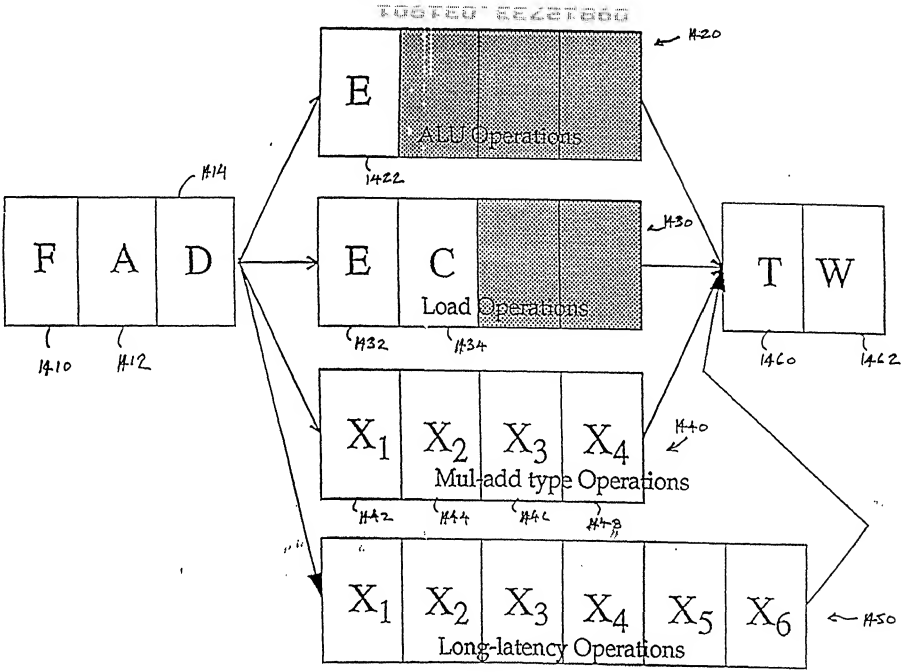

FIGURE 14 .Pipeline diagram.